Specifically, the February 6, 2003 Office Action states at page 5, paragraph 4:

> "Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. Accordingly, **THIS ACTION IS MADE FINAL.**"

This action of the Examiner is in error. NO AMENDMENTS HAVE BEEN EARLIER PRESENTED BY APPLICANTS. The last-filed response submitted on January 7, 2003 to the September 23, 2002 Office Action made no amendments of the claims - a Declaration Under 37 CFR §1.131 was submitted to overcome the rejections in the September 23, 2002 Office Action. In response, the Examiner withdrew the prior grounds of rejection, and in the current Office Action of February 6, 2003, the Examiner has introduced entirely new references as a basis for rejection.

Final rejection therefore is improper under the provisions of MPEP §706.07(a). It therefore is requested that the finality of the rejection be withdrawn.

II. Amendment of Claims

Please amend the claims as set out in **Section III** (Amended Claims) beginning on the following page.

Section III. (Amended Claims)

Amend claims 1, 2 and 30 as set out below in the listing of pending claims 1-39.

1. (Currrently amended): A microelectronic structure comprising:

at least one layer of high dielectric constant material;

at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, ~~binary metal nitrides, ternary metal nitrides,~~ TaN, NbN, HfN, ZrN, WN, W_2N, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof;

at least one metal layer in contact with the conductive barrier layer, wherein said metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu and Al;

wherein said at least one conductive barrier layer is between said at least one layer of high dielectric constant material and said at least one metal layer;

wherein when said material of said at least one metal layer is Al, said at least one material of said conductive barrier layer is not Ir or IrO_2.

2. (Currently amended): A microelectronic structure according to claim 1, wherein said ~~binary metal nitrides and ternary metal nitrides are~~ conductive barrier layer comprises at least one material selected from the group consisting of TaN, NbN, HfN, ZrN, WN, W_2N, ~~TiN, TiSiN,~~ TiAlN, TaSiN, and NbAlN.

3. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TiAlN.

4. (Original): A microelectronic structure according to claim 1, wherein said metal layer comprises Cu or Cu alloy.

5. (Original): A microelectronic structure according to claim 1, wherein said metal layer comprises Al or Al alloy.

6. (Original): A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises a complex metal oxide selected from the group consisting of $SrBi_2Ta_2O_9$ (SBT), $(Ba,Sr)TiO_3$ (BST), $BiTaO_4$ (BT), and $Pb(Zr,Ti)O_3$ (PZT).

7. (Original): A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises perovskite BST material.

8. (Original): A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises amorphous BST material.

9. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 1nm to about 100nm.

10. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 5nm to about 20nm.

11. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Pt.

12. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ir.

13. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises IrO_2.

14. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ru.

15. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises RuO_2.

16. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TiAlN.

17. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TaN.

18. (Original): A microelectronic structure according to claim 1, comprising a first conductive barrier layer and a second conductive barrier layer, wherein the first conductive barrier layer is in contact with the layer of high dielectric constant material, and the second conductive barrier layer overlies said first conductive barrier layer and is in contact with the metal layer.

19. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises IrO_2.

20. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises TiAlN.

21. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises Ir.

22. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises IrO_2.

23. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises TiAlN.

24. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises IrO_2, and said second conductive barrier layer comprises Ir.

25. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises IrO_2, and said second conductive barrier layer comprises TiAlN.

26. (Original): A microelectronic structure according to claim 1, comprising a first conductive barrier layer, a second conductive barrier layer, and a third conductive barrier layer, wherein said first conductive barrier layer is in contact with the layer of high dielectric constant material, said second conductive barrier layer overlies said first conductive barrier layer, and said third conductive barrier layer overlies said second conductive barrier layer and is in contact with the metal layer.

27. (Original): A microelectronic structure according to claim 26, wherein said first conductive barrier layer comprises IrO_2, said second conductive barrier layer comprises Ir_2O_3, and said third conductive barrier layer comprises Ir.

28. (Original): A microelectronic structure according to claim 1, comprising:

at least one layer of perovskite BST material;

a first conductive barrier layer in contact with the layer of perovskite BST material, and comprising Pt;

a second conductive barrier layer overlaying said first conductive barrier layer, and comprising Ir; and

at least one metal layer in contact with said second conductive barrier layer, comprising Cu or Cu alloy.

29. (Original): A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous BST material;

a conductive barrier layer in contact with the layer of amorphous BST material, comprising at least one material selected from the group consisting of Ir, Ru, RuO_2, and IrO_2;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

30. (Currently amended): A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous SBT material;

a conductive barrier layer in contact with the layer of amorphous SBT material, comprising at least one material selected from the group consisting of Ir, Ru, TaN, ~~TiN~~ and TiAlN;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

31. (Original): A microelectronic structure according to claim 1, comprising:

at least one layer of PZT material;

a conductive barrier layer in contact with the layer of PZT material, comprising at least one material selected from the group consisting of Ir, Ru, RuO_2, and IrO_2;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

32. (Original): A microelectronic structure according to claim 1, comprising a capacitor structure selected from the group consisting of stack capacitors and trench capacitors.

33. (Original): A microelectronic structure according to claim 1, comprising a memory cell integrated circuit structure.

34. (Original): A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a non-volatile memory cell integrated circuit structure.

35. (Original): A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a dynamic random access memory cell integrated circuit structure.

36. (Original): A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises a decoupling circuit.

37. (Original): A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an impedance matching circuit.

38. (Original): A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an analog circuit component.

39. (Original): A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an active circuit element selected from the group consisting of electrically tunable capacitor, sensor, and microelectromechanical machine MEMS).

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Claims

[c1] What is claimed is:

1.A microelectronic structure comprising:

at least one layer of high dielectric constant material;

at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from the group consisting of Pt, Ir, IrO_2, Ir_2O_3, Ru, RuO_2, binary metal nitrides, ternary metal nitrides, and compatible combinations, mixtures and alloys thereof;

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at least one metal layer in contact with the conductive barrier layer, wherein said metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu and Al.

[c2] 2.A microelectronic structure according to claim 1, wherein said binary metal nitrides and ternary metal nitrides are selected from the group consisting of TaN, NbN, HfN, ZrN, WN, W_2N, TiN, TiSiN, TiAlN, TaSiN, and NbAlN.

[c3] 3.A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TiAlN.

[c4] 4.A microelectronic structure according to claim 1, wherein said metal layer comprises Cu or Cu alloy.

[c5] 5.A microelectronic structure according to claim 1, wherein said metal layer comprises Al or Al alloy.

[c6] 6.A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises a complex metal oxide selected from the group consisting of $SrBi_2Ta_2O_9$ (SBT), $(Ba,Sr)TiO_3$ (BST), $BiTaO_4$ (BT), and $Pb(Zr,Ti)O_3$ (PZT).

[c7] 7.A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises perovskite BST material.

[c8] 8.A microelectronic structure according to claim 1, wherein said layer of high

dielectric constant material comprises amorphous BST material.

[c9] 9.A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 1nm to about 100nm.

[c10] 10.A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 5nm to about 20nm.

[c11] 11.A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Pt.

[c12] 12.A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ir.

[c13] 13.A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises IrO_2.

[c14] 14.A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ru.

[c15] 15.A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises RuO_2.

[c16] 16.A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TiAlN.

[c17] 17.A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TaN.

[c18] 18.A microelectronic structure according to claim 1, comprising a first conductive barrier layer and a second conductive barrier layer, wherein the first conductive barrier layer is in contact with the layer of high dielectric constant material, and the second conductive barrier layer overlies said first conductive barrier layer and is in contact with the metal layer.

[c19] 19.A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier

layer comprises IrO_2.

[c20] 20.A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises TiAlN.

[c21] 21.A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises Ir.

[c22] 22.A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises IrO_2.

[c23] 23.A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises TiAlN.

[c24] 24.A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises IrO_2, and said second conductive barrier layer comprises Ir.

[c25] 25.A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises IrO_2, and said second conductive barrier layer comprises TiAlN.

[c26] 26.A microelectronic structure according to claim 1, comprising a first conductive barrier layer, a second conductive barrier layer, and a third conductive barrier layer, wherein said first conductive barrier layer is in contact with the layer of high dielectric constant material, said second conductive barrier layer overlies said first conductive barrier layer, and said third conductive barrier layer overlies said second conductive barrier layer and is in contact with the metal layer.

[c27] 27.A microelectronic structure according to claim 26, wherein said first conductive barrier layer comprises IrO_2, said second conductive barrier

layer comprises Ir_2O_3, and said third conductive barrier layer comprises Ir.

[c28] 28.A microelectronic structure according to claim 1, comprising:

at least one layer of perovskite BST material;

a first conductive barrier layer in contact with the layer of perovskite BST material, and comprising Pt;

a second conductive barrier layer overlaying said first conductive barrier layer, and comprising Ir; and

at least one metal layer in contact with said second conductive barrier layer, comprising Cu or Cu alloy.

[c29] 29.A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous BST material;

a conductive barrier layer in contact with the layer of amorphous BST material, comprising at least one material selected from the group consisting of Ir, Ru, RuO_2, and IrO_2;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

[c30] 30.A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous SBT material;

a conductive barrier layer in contact with the layer of amorphous SBT material, comprising at least one material selected from the group consisting of Ir, Ru, TaN, TiN and TiAlN;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

[c31] 31.A microelectronic structure according to claim 1, comprising:

at least one layer of PZT material;

a conductive barrier layer in contact with the layer of PZT material, comprising at least one material selected from the group consisting of Ir, Ru, RuO_2, and IrO_2;

at least one metal layer in contact with the conductive barrier layer,

comprising Cu or Cu alloy.

[c32] 32.A microelectronic structure according to claim 1, comprising a capacitor structure selected from the group consisting of stack capacitors and trench capacitors.

[c33] 33.A microelectronic structure according to claim 1, comprising a memory cell integrated circuit structure.

[c34] 34.A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a non-volatile memory cell integrated circuit structure.

[c35] 35.A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a dynamic random access memory cell integrated circuit structure.

[c36] 36.A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises a decoupling circuit.

[c37] 37.A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an impedance matching circuit.

[c38] 38.A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an analog circuit component.

[c39] 39.A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an active circuit element selected from the group consisting of electrically tunable capacitor, sensor, and microelectromechanical machine MEMS).